CLAIMS

What is claimed:

1. A method for fabricating a chip-scale package, comprising:

positioning a sacrificial substrate adjacent to a back side of a device substrate with a plurality of conductive elements on an active surface of said sacrificial substrate being aligned along at least one street between adjacent semiconductor devices on an active surface of said device substrate;

securing said active surface of said sacrificial substrate to said back side of said device substrate with a quantity of dielectric material electrically isolating each conductive element of said plurality of conductive elements from said back side of said device substrate;

severing said device substrate to physically separate said adjacent semiconductor devices from one another and to form peripheral edges of each semiconductor device of said adjacent semiconductor devices, relative positions of said adjacent semiconductor devices being maintained by said sacrificial substrate;

forming a dielectric coating on at least portions of at least some of said peripheral edges;

exposing at least portions of at least some conductive elements of said plurality of conductive elements, each exposed conductive element comprising a lower section of a contact pad of the chip-scale package; and

forming a peripheral section of said contact pad in communication with a corresponding lower section and on a peripheral edge of a semiconductor device.

2. The method of claim 1, further comprising:

forming a redistribution layer on said active surface of said device substrate and in electrical isolation from circuitry of an underlying semiconductor device.

3. The method of claim 2, wherein said forming said dielectric coating includes forming a dielectric coating over at least portions of said active surface of said device substrate.

4. The method of claim 3, wherein said dielectric coating over at least portions of said active surface of said device substrate electrically isolates at least one conductive trace of said redistribution layer from circuitry of an underlying semiconductor device.

5. The method of claim 2, wherein said forming said redistribution layer is effected before said severing.

6. The method of claim 5, wherein said severing includes severing at least one conductive trace of said redistribution layer.

7. The method of claim 2, further comprising:

forming an upper section of said contact pad in communication with both said peripheral section and a conductive trace of said redistribution layer and over at least one semiconductor device of said adjacent semiconductor devices.

8. The method of claim 1, further comprising:

forming an upper section of said contact pad in communication with said peripheral section and over at least one semiconductor device of said adjacent semiconductor devices.

9. The method of claim 1, further comprising:

removing at least a portion of said sacrificial substrate to facilitate separation of said adjacent semiconductor devices from one another.

10. The method of claim 9, wherein said removing comprises substantially removing said sacrificial substrate.

11. The method of claim 10, wherein said substantially removing comprises back grinding said sacrificial substrate.

12. The method of claim 1, wherein said securing comprises use of a dielectric adhesive material.

13. The method of claim 1, wherein said severing is effected into said dielectric material.

14. The method of claim 1, wherein said forming said dielectric coating comprises introducing dielectric material into at least one recess formed during said severing.

15. The method of claim 14, wherein said introducing comprises forming a layer comprising said dielectric material over at least a portion of said active surface of said device substrate.

16. The method of claim 14, wherein said introducing comprises introducing a dielectric polymer into said at least one recess.

17. The method of claim 14, wherein said introducing comprises substantially filling said at least one recess with said dielectric material.

18. The method of claim 17, further comprising severing said dielectric material to re-separate said adjacent semiconductor devices from one another.

19. The method of claim 18, wherein said exposing is effected substantially concurrently with said severing said dielectric material.

20. The method of claim 1, wherein said positioning comprises positioning said device substrate such that said at least one street is aligned over at least some conductive elements of said plurality of conductive elements.

21. The method of claim 20, wherein said exposing comprises severing said at least some conductive elements.

22. The method of claim 1, wherein said positioning comprises positioning said device substrate such that said at least one street is aligned between an adjacent pair of conductive elements of said plurality of conductive elements.

23. The method of claim 1, further comprising:
forming a temporary protective layer over at least a portion of each of said adjacent semiconductor devices prior to said forming said dielectric coating.

24. The method of claim 23, wherein said forming said temporary protective layer is effected prior to said severing.

25. The method of claim 23, wherein said forming said temporary protective layer comprises forming said temporary protective layer over an optical element comprising at least one of a sensing area and an emission area of each semiconductor device of said adjacent semiconductor devices.

26. The method of claim 25, further comprising:
forming a redistribution layer over said active surface, at least one conductive trace of said redistribution layer extending at least partially over at least one semiconductor device of said adjacent semiconductor devices.

27. The method of claim 25, further comprising:
removing said temporary protective layer.

28. The method of claim 27, further comprising:
positioning an optically transparent lid over said optical element of at least one semiconductor device of said adjacent semiconductor devices.

29. The method of claim 28, wherein said positioning said optically transparent lid comprises positioning an optically transparent lid over optical elements of a plurality of said adjacent semiconductor devices.

30. The method of claim 29, further comprising:
severing said optically transparent lid to form an individual optically transparent lid over each of said optical elements.

31. The method of claim 30, wherein said severing said optically transparent lid is effected substantially concurrently with said exposing at least portions of at least some conductive elements.

32. The method of claim 30, wherein said severing said optically transparent lid comprises forming said individual optically transparent lid to include a peripheral edge that comprises at least one of a bevel and a chamfer.

33. The method of claim 30, wherein said forming said dielectric coating comprises severing dielectric material within at least one recess between said adjacent semiconductor devices following said severing said optically transparent lid.

34. The method of claim 28, wherein said positioning said optically transparent lid comprises positioning an individual optically transparent lid over at least said optical element of said at least one semiconductor device, said individual optically transparent lid not extending over another semiconductor device of said adjacent semiconductor devices.

35. The method of claim 28, further comprising:
forming a sacrificial layer over said optically transparent lid.

36. The method of claim 35, wherein said forming said peripheral section of said contact pad comprises:

forming a layer comprising conductive material over said sacrificial layer and on said peripheral edge;

patterning said layer comprising conductive material to form said peripheral section; and

removing said sacrificial layer and portions of said layer comprising conductive material that remain thereon.

37. The method of claim 36, wherein said removing comprises lifting said portions off of said optically transparent lid.

38. A chip-scale package, comprising:

a semiconductor device;

a redistribution layer over an active surface of said semiconductor device;

a peripheral dielectric coating covering at least a portion of an outer periphery of said semiconductor device;

at least one contact including at least one section on said peripheral dielectric coating and at least another section extending at least partially over a major surface of said semiconductor device.

39. The chip-scale package of claim 38, wherein said at least another section comprises an upper section located over a portion of said active surface of said semiconductor device.

40. The chip-scale package of claim 39, wherein said at least one contact further comprises a lower section located over a portion of a back side of said semiconductor device.

41. The chip-scale package of claim 38, wherein said at least another section comprises a lower section located over a portion of a back side of said semiconductor device.

42. The chip-scale package of claim 38, comprising at least one of a sensing area and an emission area on said active surface of said semiconductor device.

43. The chip-scale package of claim 42, further comprising an optically transparent lid covering at least said sensing area or said emission area.

44. The chip-scale package of claim 43, wherein said optically transparent lid is secured over said active surface with an optical grade adhesive.

45. The chip-scale package of claim 44, wherein said at least another section of said at least one contact pad extending at least partially over said major surface of said semiconductor device comprises an upper section of said at least one contact pad located over said active surface of said semiconductor device.

46. The chip-scale package of claim 45, wherein said upper section is exposed laterally beyond said optically transparent lid.

47. The chip-scale package of claim 45, wherein said at least one contact pad also includes a lower section located over a back side of said semiconductor device.

48. The chip-scale package of claim 43, wherein said optically transparent lid includes chamfered edges.

49. A sacrificial substrate for use in fabricating chip-scale packages, comprising:
a substantially planar substrate element; and
a plurality of contacts on a major surface of said substantially planar substrate element, each contact of said plurality of contacts being located so as to align with a street positioned between adjacent semiconductor devices on a device substrate to be assembled with the sacrificial substrate.

50. The sacrificial substrate of claim 49, wherein each contact of said plurality of contacts is located so as to be positioned beneath said street.

51. The sacrificial substrate of claim 49, wherein said plurality of contacts includes at least one pair of contacts, said at least one pair being spaced apart from one another at most a distance across said street, said contacts of said at least one pair being located so as to be positioned on opposite sides of said street.

52. An assembly for use in fabricating a plurality of chip-scale packages, comprising:
a sacrificial substrate including a plurality of conductive elements on an upper surface thereof;
a dielectric adhesive on said upper surface of said sacrificial substrate; and
a device substrate including a back side secured to said upper surface of said sacrificial substrate by said dielectric adhesive, said device substrate including adjacent semiconductor devices on an active surface thereof and at least one street between said adjacent semiconductor devices, said at least one street being positioned substantially over said plurality of conductive elements.

53. The assembly of claim 52, wherein said at least one street is positioned substantially centrally over said plurality of conductive elements.

54. The assembly of claim 52, wherein said at least one street is aligned between adjacent pairs of said plurality of conductive elements.

55. The assembly of claim 52, further comprising:
at least one optically transparent lid over said active surface of said device substrate and substantially covering an optical element thereof.

56. The assembly of claim 55, wherein said at least one optically transparent lid covers optical elements of a plurality of semiconductor devices of said adjacent semiconductor devices.

57. The assembly of claim 52, further comprising at least one recess formed along said at least one street and defining opposed peripheral edges of said adjacent semiconductor devices.

58. The assembly of claim 57, wherein a dielectric coating covers at least a portion of at least one peripheral edge of said opposed peripheral edges.

59. The assembly of claim 58, further comprising a plurality of peripheral contacts on said dielectric coating, each peripheral contact of said plurality of peripheral contacts in electrical communication with a corresponding circuit of a semiconductor device by which said peripheral contact is carried.

60. The assembly of claim 59, wherein said peripheral contact is in electrical communication with a corresponding conductive element of said plurality of conductive elements.

61. The assembly of claim 60, wherein said corresponding conductive element forms a lower section of a contact of which said peripheral contact is a part.

62. A semiconductor device assembly, comprising:

a semiconductor device component including a plurality of contacts on an upper surface thereof; and

a chip-scale package oriented at least partially over said semiconductor device component with a back side of said chip-scale package facing said upper surface of said semiconductor device component, said chip-scale package including a plurality of contacts corresponding to said plurality of contacts of said semiconductor device component, at least some contacts of said plurality of contacts including at least peripheral sections on an outer periphery of said chip-scale package; and

intermediate conductive elements disposed between at least some contacts of said plurality of contacts of said chip-scale package and corresponding contacts of said plurality of contacts of said semiconductor device component.

63. The semiconductor device assembly of claim 62, wherein said corresponding contacts of said semiconductor device component are exposed beyond said outer periphery of said chip-scale package and said intermediate conductive elements are disposed between said peripheral sections of said at least some contacts and said corresponding contacts.

64. The semiconductor device assembly of claim 62, wherein said corresponding contacts of said semiconductor device component are located beneath said chip-scale package and said intermediate conductive elements are positioned between lower sections of said at least some contacts extending over portions of a back side of said chip-scale package and said corresponding contacts.

65. A method for assembling a chip-scale package with another semiconductor device component, comprising:

orienting the chip-scale package at least partially over an upper surface of the another semiconductor device component with a back side of the chip-scale package facing said upper surface of the another semiconductor device component, the chip-scale package including a plurality of contacts corresponding to a plurality of contacts of the semiconductor device component, at least some contacts of said plurality of contacts of the chip-scale package including at least peripheral sections on an outer periphery of the chip-scale package; and

disposing intermediate conductive elements between at least some contacts of said plurality of contacts of the chip-scale package and corresponding contacts of said plurality of contacts of the semiconductor device component.

66. The method of claim 65, wherein said orienting comprises orienting the chip-scale package at least partially over said upper surface of the another semiconductor device component such that said corresponding contacts of the another semiconductor device component are exposed beyond said outer periphery of the chip-scale package and said disposing comprises disposing said intermediate conductive elements between said peripheral sections of said at least some contacts and said corresponding contacts.

67. The method of claim 65, wherein said orienting comprises orienting the chip-scale package at least partially over said upper surface of the another semiconductor device component such that said corresponding contacts of the another semiconductor device component are located beneath the chip-scale package and said disposing comprises disposing said intermediate conductive elements between lower sections of said at least some contacts extending over portions of a back side of the chip-scale package and said corresponding contacts.